IN THE SPECIFICATION

(1) Please replace the paragraph entitled "Cross Reference to Related Applications" beginning at line 2, page 1 with the following rewritten paragraph:

CROSS REFERENCE TO RELATED APPLICATIONS

The present invention is related to the following U.S. Patent Applications which are incorporated herein by reference:

~~Serial No. _____ (Attorney Docket No. AUS920000517US1) entitled "Multiphase Serializer" filed _____.~~

Serial No. [[_____]] 09/820,512 ~~(Attorney Docket No. AUS920000511US1)~~ entitled "Synchronization State Detector" filed March 29, 2001 [[_____]].

(2) Please replace the paragraph beginning at line 11, page 5 with the following rewritten paragraph:

Figures 4A and 4B ~~illustrates~~ illustrate an embodiment of the present invention of a retiming mechanism;

(3) Please replace the paragraph beginning at line 13, page 5 with the following rewritten paragraph:

~~Figure 5~~ Figures 5A-B ~~is~~ are a timing diagram illustrating the timing of the serial data, the phases of a clock and the retimed data according to the present invention; and

(4) Please replace the paragraph beginning at line 4, page 9 with the following rewritten paragraph:

Referring to Figure 4B, flip-flops 403 are configured to sample serial data 201 at an edge, e.g., negative edge, of a particular phase, e.g., Ø1. For example, flip-flop 403A may be configured to receive as inputs phase Ø1, the complement of phase Ø1 (Ø1B) and serial data 201 thereby being able to sample serial data 201 using an edge, e.g., negative edge, of phase Ø1. Flip-flop 403B may be configured to receive as inputs phase Ø2, the complement of phase Ø2 (Ø2B) and serial data 201 thereby being able to sample serial data 201 using an edge, e.g., negative edge, of phase Ø2. Flip-flop 403C may be configured to receive as inputs phase Ø3, the complement of phase Ø3 (Ø3B) and serial data 201 thereby being able to sample serial data 201 using an edge, e.g., negative edge, of phase Ø3. Flip-flop 403D may be configured to receive as inputs phase Ø4, the complement of phase Ø4 (Ø4B) and serial data 201 thereby being able to sample serial data 201 using an edge, e.g., negative edge, of phase Ø4. Flip-flop 403E may be configured to receive as inputs phase Ø5, the complement of phase Ø5 (Ø5B) and serial data 201 thereby being able to sample serial data 201 using an edge, e.g., negative edge, of phase Ø5.

(5) Please replace the paragraph beginning at line 3, page 6 with the following rewritten paragraph:

Figure 1 illustrates an embodiment of the present invention of a serial data link 100 used in a communication system. As stated in the Background Information, data may typically be transmitted between various devices in a communication system through a data link. Typically, data is transmitted in parallel whenever possible in order to increase bandwidth. However, due to cost, weight, interference (noise) and electrical loading considerations, parallel transmission is not feasible in many systems. In order to simplify the communications problem, data may be transmitted serially across a serial data link 100 by a transmitter 101. Transmitter 101

may be configured to convert the parallel data to a serial form which may be transmitted through a medium 102, e.g., wired, wireless, to a receiver 103 configured to convert the serial data into parallel form which may then be transmitted to another device, e.g., computer, cellular phone. ~~A more detailed discussion of transmitter 101 converting parallel data into serial data using multiple phases of a clock at a frequency lower than the serial data rate is described in detail in U.S. Application No. _____, filed on _____, entitled "Multiphase Serializer," Attorney Docket No. AUS920000517US1, which is hereby incorporated herein by reference in its entirety.~~

(6) Please replace the paragraph beginning at line 18, page 11 with the following rewritten paragraph:

As stated above, a particular transmission gate, e.g., 404C, may be activated based upon the logical states of the inputs as determined by the combinational logic, e.g., plurality of NAND gates 401 and a plurality of inverters 402, in retiming mechanism as illustrated in ~~Figure 5~~ Figure 4A.

(7) Please replace the paragraph beginning at line 22, page 11 with the following rewritten paragraph:

~~Figure 5~~ Figures 5A-B – Timing Diagram

~~Figure 5 is~~ Figures 5A-B are a timing diagram that illustrate[[s]] the timing of serial data 201, the phases of the clock generated by oscillator 202 as well as the retimed data where the retimed data is the serial data signal 201 with diminished timing uncertainties.

(8) Please replace the paragraph beginning at line 1, page 12 with the following rewritten paragraph:

For example, at the point in time at T1, phase Ø3 is the appropriate phase to use to sample the serial data signal 201 since the falling edge of phase Ø3 is aligned with the point in time at T1. Referring to Figures 4A, 4B, 5A and 5B ~~and 5~~, when the logical state of phase Ø3 becomes low, flip-flop 403C sampling the serial data signal 201 using phase Ø3 of the clock generated by oscillator 202 outputs the sampled serial data signal 201 to A3. The value of the sampled serial data signal 201 at A3 will be outputted to node 405 when the logical state of C3 is low and the logical state of B3 is high thereby activated transmission gate 404C. The logical state of C3 is low and the logical state of B3 is high when the inputs to NAND gate 401C, Ø4B and Ø5, are both high. That is, the logical state of C3 is low and the logical state of B3 is high when the logical state of phase Ø4 is low and the logical state of phase Ø5 is high. That occurs during the shaded region labeled "A" as illustrated in Figure 5A. The value of the sampled serial data signal 201 at A3 that was outputted to node 405 upon activation of transmission gate 404C subsequently becomes part of the retimed_data as illustrated in Figure 5A at the point in time at T3.

(9) Please replace the paragraph beginning at line 16, page 12 and ending at line 2, page 13 with the following rewritten paragraph:

At the point in time at T2, phase Ø4 is the appropriate phase to use to sample the serial data signal 201 since the falling edge of phase Ø4 is aligned with the point in time at T2. Referring to Figures 4A, 4B, 5A and 5B ~~and 5~~, when the logical state of phase Ø4 becomes low, flip-flop 403D sampling the serial data signal 201 using phase Ø4 of the clock generated by oscillator 202 outputs the sampled serial data signal 201 to A4. The value of the sampled serial data signal 201 at A4 will be outputted to node 405 when the logical state of C4 is low and the logical state of B4 is high thereby activated transmission gate 404D. The logical state of C4 is low and the logical state of B4 is high when the inputs to NAND gate 401D, Ø5B and Ø1, are both high. That is, the logical state of C4 is low and the logical state of B4 is high when the logical state of phase Ø5 is low and the logical state of phase Ø1 is high.

That occurs during the shaded region labeled "B" as illustrated in Figure 5A. The value of the sampled serial data signal 201 at A4 that was outputted to node 405 upon activation of transmission gate 404D subsequently becomes part of the retimed_data as illustrated in Figure 5A at the point in time at T4.

(10) Please replace the term "**CLAIMS:**" beginning at line 1, page 15 with the following:

We Claim: